CLEAN VERSION OF AMENDED CLAIMS

1. (Twice amended) A method for forming a super self-aligned bipolar transistor, comprising the steps of:

providing a semiconductor substrate having a buried collector region;

providing multiple layers above said collector region;

providing an emitter window mask above said multiple layers;

providing three vertical etchings of said multiple layers;

providing a doping of said collector region wherein the doped collector region is determined by the emitter window mask;

providing a horizontal etching of one of said multiple layers, wherein said horizontally etched layer is a polysilicon layer and is etched a distance greater than a thickness of said polysilicon layer;

providing a wet etching to remove a final one of said multiple layers;

providing a base region above said collector region in the horizontally etched area; and

providing an emitter region above the base region so that the emitter, base and collector regions are super self-aligned wherein said horizontal etching determines that a dimension of said base region is wider than a dimension of said doped collector region and a dimension of said emitter region.

8. (Twice amended) A super self-aligned bipolar transistor, comprising:

a semiconductor substrate having a buried collector region;

multiple layers above said collector region;

an emitter window mask above said multiple layers;

a doped collector region wherein the width of the doped collector region are equal to the emitter window mask width;

a horizontal etched region of one of said multiple layers, wherein said horizontally etched region is a polysilicon region and extends a distance greater than a thickness of said polysilicon region;

a base region above said collector region in the horizontally etched area; and

an emitter region above the base region so that the emitter, base and collector regions are super self-aligned wherein said horizontally etched region determines that a dimension of said base region is wider than a dimension of said doped collector region and a dimension of said emitter region.

10. (Once amended) The apparatus as described in claim 10 further comprising an oxide surface and a Nitride layer above said layers of surface oxide and polysilicon.

18. (Twice amended) A method for forming a super self-aligned bipolar transistor, comprising the steps of:

providing a semiconductor substrate having a buried collector region;

providing a first oxide layer, a polysilicon layer and a second oxide layer above said collector region;

providing a Nitride emitter window mask above said oxide and polysilicon layers;

providing a wet etching with hydrofluoric acid solutions to etch first and second oxide layers;

providing a doping of said collector region wherein the doped collector region is determined by the emitter window mask;

providing a horizontal etching of said polysilicon layer, wherein said horizontal etching is etched a distance greater than a thickness of said polysilicon layer;

providing a base region above said collector region in the horizontally etched area wherein the base region extends horizontally beyond the doped collector region; and

providing an emitter region above the base region so that the emitter, base and collector regions are super self-aligned wherein said horizontal etching determines that a dimension of said base region is wider than a dimension of said doped collector region and a dimension of said emitter region.

21. (Once amended) A method for forming a super self-aligned bipolar transistor, comprising the steps of:

providing a semiconductor substrate having a buried collector region;

providing multiple layers above said collector region;

providing an emitter window mask above said multiple layers;

providing three vertical etchings of said multiple layers;

providing a doping of said collector region wherein the doped collector region is determined by the emitter window mask;

providing a horizontal etching of one of said multiple layers, wherein said horizontal etching is performed to a distance greater than a thickness of said polysilicon and whereby said distance may be conformed to provide desired electrical characteristics;

providing a wet etching to remove a final one of said multiple layers;

providing a base region above said collector region in the horizontally etched area; and

providing an emitter region above the base region so that the emitter, base and collector regions are super self-aligned wherein said horizontal etching determines that a dimension of said base region is wider than a dimension of said doped collector region and a dimension of said emitter region.

23. (Once amended) The method of claim 21 wherein the desired electrical characteristics are transistor gain and frequency response.